Notice of Allowability	Application No.	Applicant(s)	
	10/032,789	WALTHER ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *November 3, 2005*.

2. ☒ The allowed claim(s) is/are *1,2,4,5,7-18 and 20-22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean copy of allowed claims*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated November 3, 2005. Claims 1, 5, 13 and 20 were amended. Claims 21 and 22 were added. Claims 1-22 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. David Hsia on December 22, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. The application has been amended as follows:

In Claim 1:

Replace claim 1 with:

1. A method for editing a netlist, the method comprising:

providing a version of the netlist comprising a set of hardware description language netlist modules;

creating a changes module in hardware description language describing at least one consistent change to the netlist modules, the at least one consistent change being applicable to multiple versions of the netlist;

using the changes module to modify at least one of the netlist modules according to the at least one consistent change to create a modified versions of the netlist.

In Claim 3:

Cancel Claim 3.

In Claim 6:

Cancel Claim 6.

In Claim 13:

Replace claim 13 with:

13. A method for editing a netlist, the method comprising:

providing a version of the netlist comprising a set of hardware description language netlist modules;

creating a changes module in hardware description language describing at least one consistent change to the netlist modules, the at least one consistent change including a change in

a port configuration of a wire in the netlist, the at least one consistent change being applicable to multiple versions of the netlist; and

using the changes module to modify at least one of the netlist modules according to the at least one consistent change to create a modified version of the netlist.

In Claim 19:

Cancel Claim 19.

In Claim 20:

Replace claim 20 with:

20. A computer-readable medium comprising program instructions which when executed on a computer performs a process for editing a netlist, comprising :

receiving a netlist comprising a set of hardware description language netlist modules;

receiving a changes module in hardware description language describing at least one consistent change to the netlist modules, the at least one consistent change being applicable to multiple versions of the netlist; and;

using the changes module to modify at least one of the netlist modules according to the at least one consistent change to create a modified netlist.

In Claims 21:

Replace claim 21 with:

21. The method of claim 1, further comprising:

providing another version of the netlist comprising the set of hardware description language netlist modules; and

using the changes module in hardware description language to modify at least one of the netlist modules in the another version of the netlist according to the at least one consistent change to create another modified version of the netlist.

In Claim 22:

Replace claim 22 with:

22. The method of claim 13, further comprising:

providing another version of the netlist comprising the set of hardware description language netlist modules; and

using the changes module in hardware description language to modify at least one of the netlist modules in the another version of the netlist according to the at least one consistent change to create another modified version of the netlist.

A clean copy of the allowed claims is attached.

Reasons for Allowance

4. Claims 1-2, 4-5, 7-18, 20-22 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) A method of converting a PLD representation of a circuit into a second representation of the circuit; the user enters the text or graphic representation of the circuit design using a software tool; the design description may include a hardware description language or a netlist description of circuit design; the pre-compile representation of the PLD representation may include generating an HDL file that includes several instances of different general models; a compiler converts the pre-compile representation to a post-compile representation; the method modifies one or more delay element representations; the resulting circuit specification includes additional timing information; the netlist is edited to change the delay associated with one or more delay elements; this can be accomplished by adding or subtracting delay inducing components or substituting delay elements of different components; the modifications are made by editing netlist to modify one or more hard library elements associated with delay elements (**Baxter et al.,** U. S. Patent 6,625,787);

(2) a circuit designing apparatus, a circuit designing method and a timing distribution apparatus for designing an LSI circuit; the method uses hierarchical design in which one unit contains another unit designed independently and is at a lower level; the automatic design processing unit executes circuit designing and includes a hardware description language conversion processing section; change information of changes produced by the designing apparatus are stored to automatically produce and optimize a desired circuit; the method provides

a timing distribution apparatus for the hierarchical design; the timing distribution unit includes a logic/constraint storage section, for distributing timings based on a floor plan to perform provisional wiring line and a timing information storage section for storing netlist information; the inter-hierarchical layer association manager may update, when the timing distribution values are changed, a higher hierarchical layer entity than the hierarchical layer in which the timing distribution values are changed; the distribution manager includes a distribution editor connected to the logic/constraint information storage section for distributing timings (**Takeyama et al.,** U. S. Patent Application 2002/0083398);

(3) a method and apparatus for inserting antenna diodes into an integrated circuit design by placing design cells in an IC layout according to a netlist for the IC design; the system uses a schematic editor and a netlist modifier; a netlist in a schematic database is generated by a schematic editor module; additionally a hardware description language process may be used to generate the netlist instead of the schematic process; a netlist modifier module receives information from the antenna diode selection module and modifies the netlist to include the diode cells and their connectivity information in a modified netlist; (**Lee et al.**, U. S. Patent Application 2002/0138817); and

(4) a simulation system with a schematic editor that allows incremental changes to a design under test without requiring shutdown of the simulator; the method permits a wide range of design changes and generates a resulting netlist for the changed design; the changes in the schematic include changes in hierarchy, addition or deletion of components, signals, interconnection of components and interface ports, substitution of a new component for an existing one and alteration of parametric data such as device delay timing; the method reduces

the processing time required to perform incremental design change; a first circuit represented in a netlist is input to the simulator; the simulator produces the response values during simulation; then at least one design change is input to the in a graphical schematic editor; in response to the design change, portions of the netlist are modified and a second circuit produced; simulation is then continued with the modified netlist; the system uses graphical user interface to modify or edit a picture of the circuit (**Lazansky et al.**, U. S. Patent 5,111,413).

None of these references taken either alone or in combination with the prior art of record discloses a method for editing a netlist, specifically including:

(Claim 1) "creating a changes module in hardware description language describing at least one consistent change to the netlist modules, the at least one consistent change being applicable to multiple versions of the netlist; and using the changes module to modify at least one of the netlist modules according to the at least one consistent change to create a modified versions of the netlist".

None of these references taken either alone or in combination with the prior art of record discloses a method for editing a netlist, specifically including:

(Claim 13) "creating a changes module in hardware description language describing at least one consistent change to the netlist modules, the at least one consistent change including a change in a port configuration of a wire in the netlist, the at least one consistent change being applicable to multiple versions of the netlist; and using the changes module to modify at least

one of the netlist modules according to the at least one consistent change to create a modified version of the netlist".

None of these references taken either alone or in combination with the prior art of record discloses a computer-readable medium comprising program instructions which when executed on a computer perform a process for editing a netlist, specifically including:

(Claim 20) "receiving a changes module in hardware description language describing at least one consistent change to the netlist modules, the at least one consistent change being applicable to multiple versions of the netlist; and using the changes module to modify at least one of the netlist modules according to the at least one consistent change to create a modified netlist".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
December 22, 2005

Paul L. Rodriguez 12/23/05
Primary Examiner
Art Unit 2123